THE BELL SYSTEM TECHNICAL JOURNAL
Vol. 53, No. 8, October 1974
Printed in U.S.A.

Design Considerations for a Two-Phase, Buried-Channel, Charge-Coupled Device

By J. McKENNA, N. L. SCHRYER, and R. H. WALDEN

(Manuscript received March 29, 1974)

The design of a two-phase, buried-channel (or bulk-channel) charge-coupled device is presented. Directionality is obtained by using a stepped-oxide structure. The basic operation of the device is explained, and the effect that changes in various design parameters have on its operation is examined in some detail. A set of roughly optimal parameters are found that yield an extremely fast and efficient device. We estimate a charge-transfer time of 1.8 ns and a charge capacity of 4.1 × 10^{11} (electrons/cm²). Only existing technology is necessary for its fabrication.

This paper presents some design considerations for a two-phase, buried-channel (or bulk-channel) charge-coupled device (BCCD). The concept of the BCCD has been presented previously,[1,2] and operation of three-phase BCCD's has been demonstrated.[3–6] Two-phase surface charge-coupled devices (CCD's) have advantages over three-phase surface CCD's in many applications, and several designs have been discussed.[7–12] Therefore, it seems important and timely to consider the design of two-phase BCCD's.

We present here a brief review of the basic n-channel BCCD structure. Figure 1 shows the CCD electrode configuration originally proposed for the buried-channel device.[1] Beneath the charge-transfer electrodes are successively a layer of silicon dioxide about 1200 Å thick, a layer of n-type single-crystal silicon, and finally the substrate of lightly doped p-type silicon. By depleting the entire n-region and part of the adjacent p-substrate of mobile carriers with the aid of a reverse-biased diode at the end of the channel, a potential configuration is obtained like the one shown schematically in Fig. 2.[1] Here we plot the negative of the electrostatic potential, i.e., the potential energy of

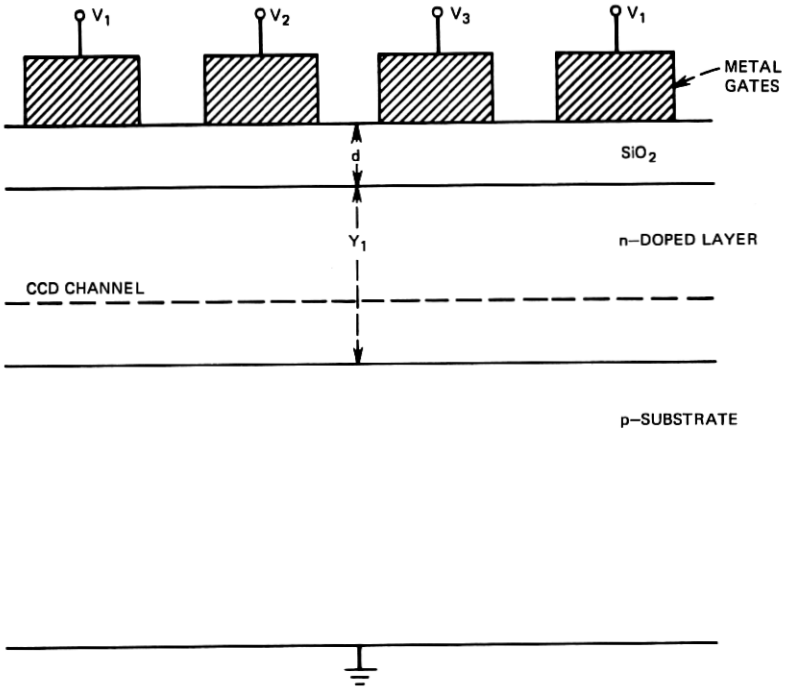

Fig. 1—Schematic diagram of a three-phase buried-channel CCD.

an electron. The distinguishing feature is that the potential energy minimum is located away from the semiconductor-insulator interface; this means that any mobile charge being transferred down the channel travels in bulk silicon, and the transfer should be free of losses associated with interface states. It also means that the free carrier mobility may have a value close to that for bulk. Both these factors were expected to increase transfer efficiency relative to surface CCD's, but at the expense of a reduced charge-carrying capability resulting from the reduced capacitance associated with the increased separation between the metal gates and the channel.

However, there are necessarily gaps between adjacent electrodes in this three-phase device. Since the image charge in the metal plays an important role in controlling the channel potential, the finite gaps give rise to local potential wells, which store charge between the electrodes.[1,13] The amount of charge in each well is not constant; it depends on the values of the clock voltages on neighboring gate electrodes. Thus, charge can be exchanged between the signal and the well. This can

lead to extremely inefficient transfer.[1] It has been shown that this problem can be eliminated by ensuring that the potential between electrodes varies monotonically as a function of distance between plates.[3,13,14] The gap problem can also be alleviated by using a fabrication procedure that reduces the interelectrode gap to zero.[15] If we have a zero-gap two-phase device, there will be operational and fabricational simplifications relative to three-phase devices.

The stepped-oxide structure illustrated in Fig. 3 not only can be operated as a two-phase BCCD, but it also has essentially zero gaps between the electrodes.[10,11] This is the basic configuration studied in this paper. Other studies of this configuration have been made.[16–18] Techniques now exist for fabricating the device. The n-type layer, which has a uniform surface concentration, can be obtained by doing an ion implant in the required channel region before the oxide steps are defined. The definition of metallization and oxide steps can be accomplished by using either the undercut isolation scheme[10] or an overlapping-gate technology.[11]

Our purposes here are to investigate the principles of operation of the device, to study the effect of varying certain of its design parameters, and to attempt to make a reasonably optimal choice of these parameters.

In Fig. 3, we see that the width of the electrode over the thick-oxide step is w_1 and over the thin-oxide step is w_2. The thickness of the thick step is d_1 and of the thin step d_2; the permittivity of the oxide

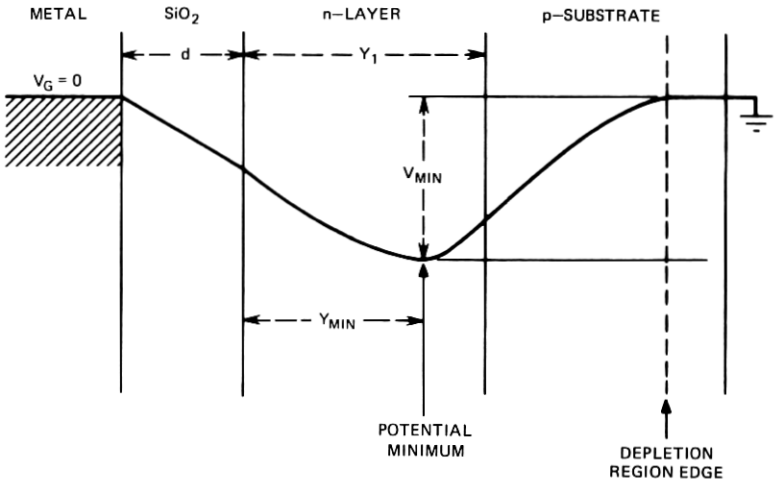

Fig. 2—Schematic potential diagram of a buried-channel CCD.

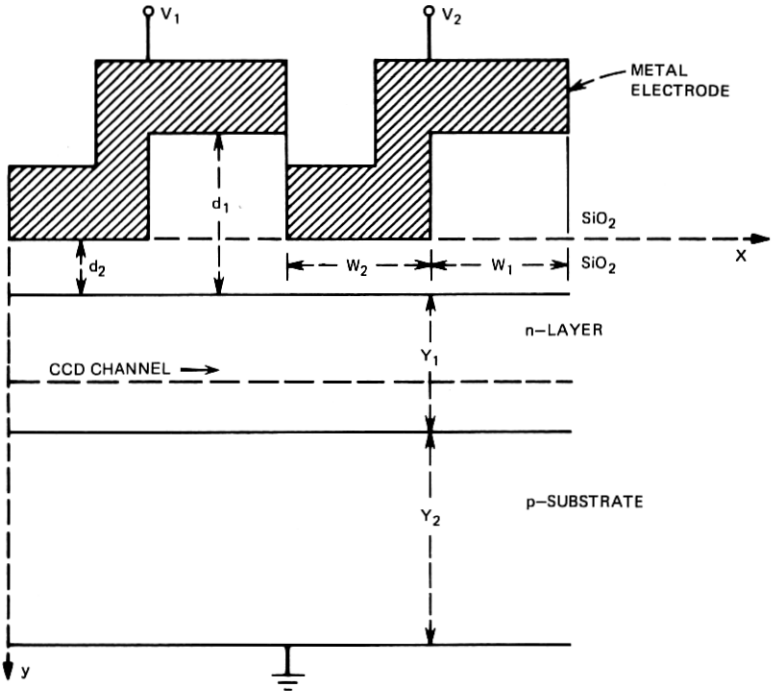

Fig. 3—Schematic diagram of a two-phase, stepped-oxide BCCD.

is ϵ_{0x}. The n-type layer has thickness Y_1 and permittivity ϵ_s, and the donor density N_D is assumed to vary with position as[19]

$$N_D(y) = c_s \exp\left\{-\left(\frac{y - d_2}{Y_1}\right)^2 \ln\frac{c_s}{N_A}\right\} - N_A, \tag{1}$$

where y is distance measured from the top of the thin-oxide step, c_s is the number density of donor ions at the upper surface of the n-type layer, and N_A is the acceptor number density of the p-type substrate. Finally, the uniformly doped p-type substrate has thickness Y_2 and permittivity ϵ_s. Of these, the design parameters are d_1, Y_1, and the total implanted charge in the n-layer.

The operation of the device can be qualitatively explained on the basis of a simplified one-dimensional model with constant n-layer doping N_D, which is discussed in the appendix. As shown there, the depth of the potential energy well, shown schematically in Fig. 2, increases with increasing oxide thickness. This means that the region under the thin oxide in Fig. 3 will act as a barrier to charge flow while that under the thick oxide will store charge. Interestingly, this is just

the opposite of the case for a surface CCD, and consequently the direction of transfer in a two-phase BCCD is opposite to that of a surface device. The device acts as a BCCD provided the electrode voltage does not exceed a limiting value V_{lim}, where

$$V_{\text{lim}} = \frac{N_D}{2N_A}\left(1 + \frac{N_D}{N_A}\right)\frac{eN_A Y_1^2}{\epsilon_s}. \tag{2}$$

If the plate voltage exceeds V_{lim}, then the potential minimum is located exactly at the insulator-semiconductor interface. Typically, V_{lim} has a value of several hundred volts.

We wish to choose the design parameter values so that the potential well under the thick oxide is deep enough to store as much signal charge as possible, and yet the potential barrier between two wells can be overcome by applying reasonable potentials to the plates to obtain complete transfer of this charge.

To obtain more quantitative information about the device, we turn to a two-dimensional calculation. We use a model described in an earlier paper[13] to calculate the electrostatic potential $\varphi(x, y)$ in the absence of any mobile charge. For the purpose of the two-dimensional

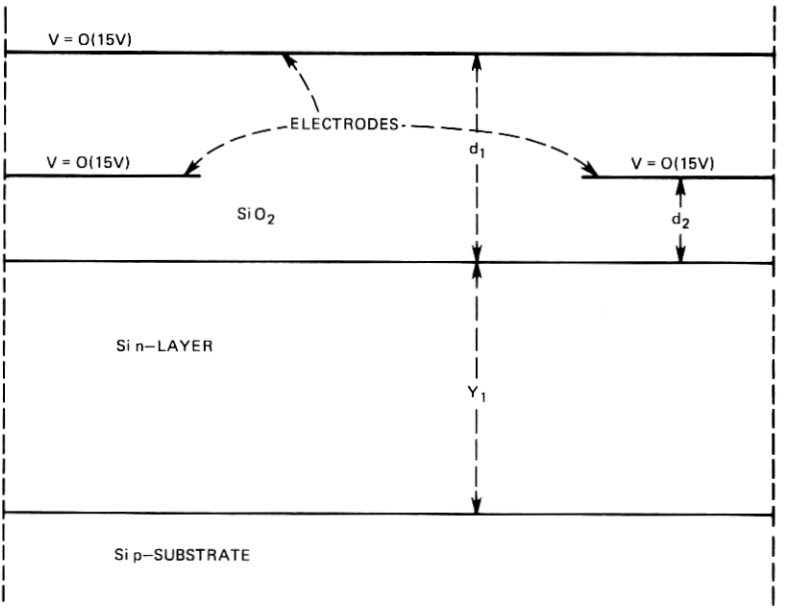

Fig. 4—Single cell of the model used to calculate curves of Figs. 5 and 6 and numbers of Table I.

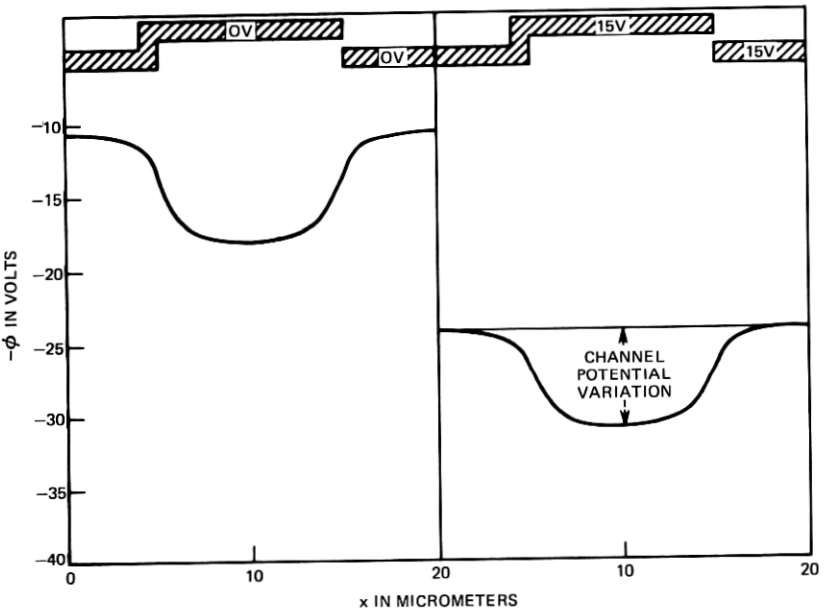

Fig. 5—Channel potential in a two-phase BCCD with all plates either at 0 or 15 volts. Parameters are $d_1 = 0.3$ μm, $d_2 = 0.12$ μm, $Y_1 = 1.2$ μm, $Q_n = 1.5 \times 10^{12}$ cm^{-2}, $N_A = 5 \times 10^{14}$ cm^{-3}.

potential calculation, the plate widths w_1 and w_2 are kept fixed at 10 μm throughout the discussion, as is the thin-oxide thickness at $d_2 = 0.12$ μm. The uniform doping of the n-type substrate is also held fixed at $N_A = 5 \times 10^{14}$ cm^{-3}, and it is assumed that $Y_2 \geqq 50$ μm, which is at least twice the maximum-depletion-region width at any voltage considered. These values are similar to those commonly used in most MOS technologies. We somewhat arbitrarily put an upper limit of 15 volts on the potential difference between electrodes, which we are willing to use to transfer charge from one potential well to a neighboring one.

First, we consider the case in which the electrodes are all at the same potential, either 0 or 15 volts, and we approximately model the device by the configuration in Fig. 4. The potentials and fields were calculated for combinations of the following parameter values: thick-oxide thicknesses (d_1) of 0.3 and 0.6 μm; n-layer thicknesses (Y_1) of 0.4 and 1.2 μm, and total n-layer doping charges (Q_n) of 0.5×10^{12} cm^{-2}, 1.5×10^{12} cm^{-2}, and 4.5×10^{12} cm^{-2}. The spatial distribution of doping in the n-layer is assumed to be given by (1). It can be shown[20]

that c_s, Y_1, and Q_n are related by

$$Q_n = Y_1 \left\{ \frac{\sqrt{\pi}}{2} \left\{ \frac{c_s}{\sqrt{\ln (c_s/N_A)}} \right\} \operatorname{erf} [\sqrt{\ln (c_s/N_A)}] - N_A \right\}, \qquad (3)$$

where erf (z) is the error function.[21] Equation (3) was used to calculate c_s, given the other parameter values.

Figures 5 and 6 give plots of the channel potential $\varphi_c(x)$ as a function of distance parallel to the oxide semiconductor interface for two sets of parameter values shown in the figure captions. If $\varphi(x, y)$ is the electrostatic potential in the device, then

$$\varphi_c(x) = - \max_{d_2 \leqq y \leqq d_2 + Y_1} \varphi(x, y). \qquad (4)$$

We summarize our calculations in Table I. Of particular interest is the variation of the channel potential with the thick-oxide thickness. The variation is defined as the voltage difference between the minimum and the maximum, as shown in Figs. 5 and 6. For $Y_1 = 1.2$ μm,

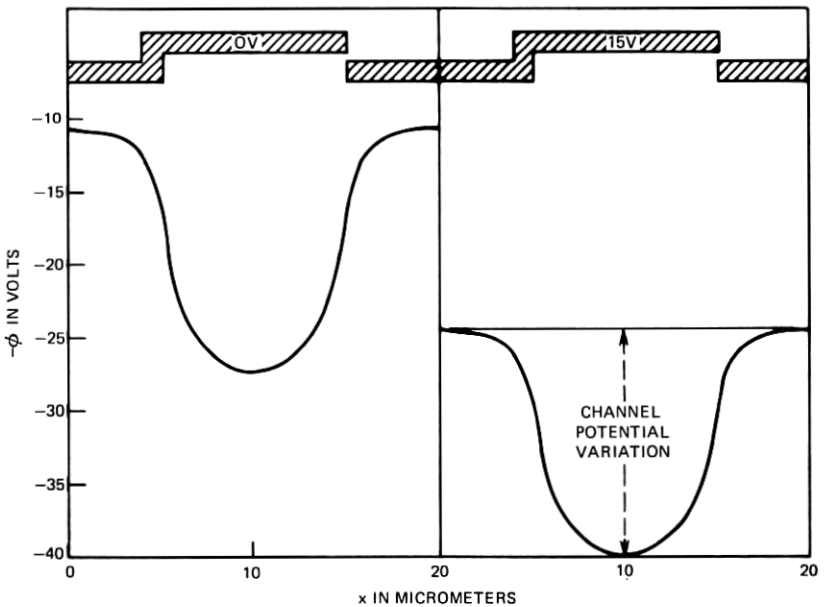

Fig. 6—Channel potential in a two-phase BCCD with all plates either at 0 or 15 volts. The parameters are $d_1 = 0.6$ μm, $d_2 = 0.12$ μm, $Y_1 = 1.2$ μm, $Q_n = 1.5 \times 10^{12}$ cm^{-2}, $N_A = 5 \times 10^{14}$ cm^{-3}.

Table I

d_1 in μm	Y_1 in μm	$10^{-12}Q_n$ in cm^{-2}	Plate Voltage in V	Minimum Channel Potential in V	Maximum Channel Potential in V	Minimum Channel Depth in μm	Plate Voltage Limit V_{lim}
0.6*	0.4	1.5	0	−25.28	−7.56	0.106	343
0.6*	0.4	1.5	15	−38.23	−22.02	0.099	343
0.3	0.4	1.5	0	−15.62	−7.93	0.140	343
0.3	0.4	1.5	15	−28.90	−21.87	0.124	343
0.6*	1.2	1.5	0	−27.27	−10.78	0.381	352
0.6*	1.2	1.5	15	−39.83	−24.51	0.340	352
0.3	1.2	1.5	0	−17.89	−10.61	0.398	352
0.3	1.2	1.5	15	−30.88	−24.23	0.398	352
0.6*	0.4	0.5	0	−6.78	−2.35	0.096	39
0.6*	0.4	0.5	15	−18.58	−16.01	0.050	39
0.3	0.4	0.5	0	−4.42	−2.34	0.125	39
0.3	0.4	0.5	15	−17.12	−15.99	0.058	39
0.6*	1.2	4.5*	0	−91.3	−35.63	0.398	3088
0.6*	1.2	4.5*	15	−104.74	−49.90	0.390	3088
0.3	1.2	4.5*	0	−58.57	−34.45	0.398	3088
0.3	1.2	4.5*	15	−72.25	−48.58	0.398	3088

* Unacceptable values.

$Q_n = 1.5 \times 10^{12}$ cm^{-2}, and a plate voltage of 15 volts, the values of the variation are 6.65, 11.75, and 15.32 volts, corresponding respectively to d_1 values of 0.3, 0.45, and 0.6 μm.

Note that the physical depth of the channel (the distance of the potential minimum below the oxide interface) is less by as much as a factor of 2 when the doping profile is given by (1) than when it is constant, equal to the average doping, which has been pointed out elsewhere.[22]

Although actual operation of the device involves having different voltages on successive electrodes, a first screening of the possible parameter values can be made on the basis of the calculations described in the preceding paragraphs. A criterion for total charge transfer from under the plate at 0 volt to the plate at 15 volts is that the minimum channel potential under the 0-volt plate be greater than the maximum channel potential under the plate at 15 volts, i.e., the barrier potential in the receiving region should be less than that of the potential well in the sending region. Table I shows that all cases of $d_1 = 0.6$ μm or $Q_n = 4.5 \times 10^{12}$ cm^{-2} violate this condition. The cases of $Q_n = 4.5 \times 10^{12}$ cm^{-2} and $Y_1 = 0.4$ μm are not shown because they would also violate this condition. These parameter choices were re-

jected. The parameter value $Q_n = 0.5 \times 10^{12}$ cm^{-2} was also rejected because the minimum channel depth is small.

There remain the parameter values $d_1 = 0.3$ μm and $Q_n = 1.5 \times 10^{12}$ cm^{-2}, and either $Y_1 = 0.4$ μm or $Y = 1.2$ μm. Since there seems to be little difference between these two cases on the basis of the calculations so far, we also consider the case in which d_1 and Q_n are as stated above and $Y_1 = 0.8$ μm. We now examine the device in which one plate is at 0 volt and the adjacent one at 15 volts. The device was modeled by the configuration of Fig. 7, and the calculations are again based on the model of Ref. 13, in which there is no mobile charge. In all the calculations to be discussed now, we took $d_1 = 0.3$ μm, $d_2 = 0.12$ μm, $Y_1 = 0.4$, 0.8, or 1.2 μm, $Q_n = 1.5 \times 10^{12}$ cm^{-2}, $N_A = 5 \times 10^{14}$ cm^{-3}, and $N_D(y)$ given by (1). Figure 8 plots some results for one cell of such a BCCD for the case $Y_1 = 0.8$ μm; φ_c is the channel potential,

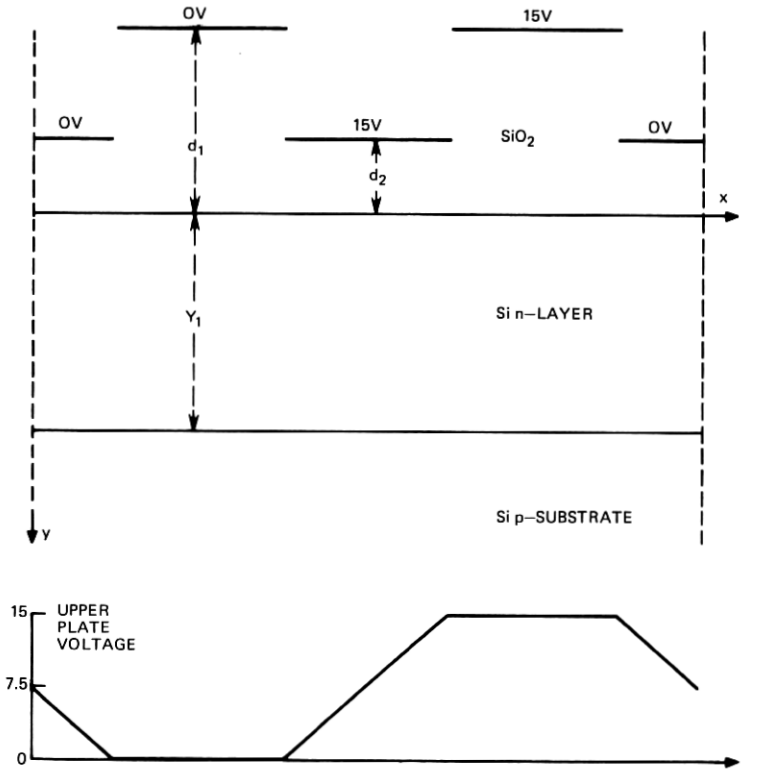

Fig. 7—Two cells of the model used to calculate the curve of Fig. 8. Assumed potential variation along the second level of metallization is shown below.

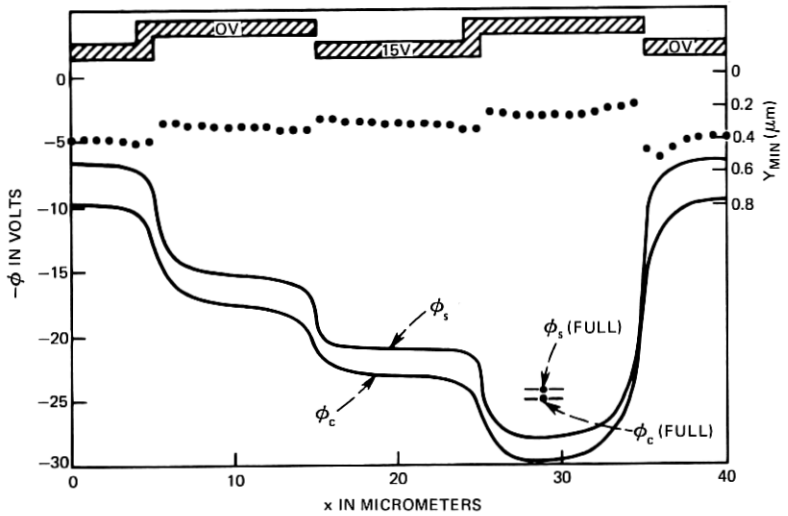

Fig. 8—Channel potential φ_c and potential at the semiconductor oxide interface φ_s in two cells of a two-phase BCCD. There is no inserted charge, plate potentials are as shown, and parameters are $d_1 = 0.3$ μm, $d_2 = 0.12$ μm, $Y_1 = 0.8$ μm, $Q_n = 1.5 \times 10^{12}$ cm^{-2}, $N_A = 5 \times 10^{14}$ cm^{-3}. The dashed curve shows the position of the channel below the oxide-semiconductor interface. φ_c and φ_s at the potential minimum under the receiving plate are also indicated when the device is full of charge.

φ_s is the potential at the oxide-semiconductor interface, and the dotted curve is the position of the potential minimum below the oxide-semiconductor interface.

The amount of charge that can be carried in this BCCD was estimated using a one-dimensional analysis in the well. Charge was added to the one-dimensional well until the minimum potential in the well just equalled the barrier potential; that is, the potential under the thin-oxide step part of the 15-volt plate of Fig. 8. The values obtained ($3–5 \times 10^{11}$ cm^{-2}) indicate that practical quantities of charge can be handled by the BCCD. The method of this calculation[23] is similar to one carried out by Kent.[24]

It is of interest to consider the relative values of surface potential and channel potential for empty and full wells. Figure 8 shows the results of the two-dimensional calculation for both potentials with no free charge; a potential difference of approximately 1.75 volts is maintained along the channel in the receiving well. As the well is filled with charge, this difference is reduced to 0.825 volt, as is indicated in the diagram. These last data were obtained with the aid of the one-dimensional calculation described above.[23] The 0.825-volt

differential ensures that the carrier concentration at the silicon-silicon-dioxide interface will be a negligible fraction of that in the channel which, in turn, indicates that device performance will be essentially unhindered by surface effects.

Table II contains a list of charge-carrying capacities and fringing field values as a function of Y_1. Notice that the capacity falls off relatively slowly with increasing Y_1, while the fringing fields increase at a somewhat more rapid rate. Two columns give field strengths; the left-hand column refers to the minimum horizontal field in the channel under the "sending" well, and the right-hand column refers to that under the "receiving" barrier. Notice that charge transport will be mainly limited by the fields under the latter. The situation would reverse if the maximum clock voltage were increased somewhat beyond the 15 volts used here. It is shown below, however, that a field strength of 710 V/cm is sufficient to ensure extremely rapid charge transfer. The data in Table II show that the ultimate choice of Y_1 is one involving a tradeoff between capacity and fringing field and would depend on the particular device requirements.

Both from the simple model in the appendix and from our two-dimensional calculations, we estimate that, for our choice of parameter values, the electric field at the semiconductor surface never exceeds 1.8×10^5 V/cm and at the p–n junction never exceeds 10^5 V/cm. These fields are below the avalanche breakdown fields for these conditions ($3–4 \times 10^5$ V/cm). It can be shown that the field at the semiconductor surface increases with increasing Q_n, so if Q_n is too large, this field will exceed the avalanche breakdown field. In fact, our calculations show that in the case $Q_n = 4.5 \times 10^{12}$ cm^{-2}, $Y_1 = 1.2$ μm, which we rejected for other reasons, the surface field is about 5.8×10^5 V/cm, which indeed exceeds the avalanche breakdown field for that case.

Finally, we estimated the speed with which the device of Fig. 8 can transfer charge from one well to the neighboring well. A technique of

Table II

Y_1 in μm	Charge Capacity in cm^{-2}	Fringe Field Under Well in V/cm	Fringe Field Under Barrier in V/cm
0.4	4.8×10^{11}	1395.	482.
0.8	4.1×10^{11}	1755.	710.
1.2	3.4×10^{11}	1955.	845.

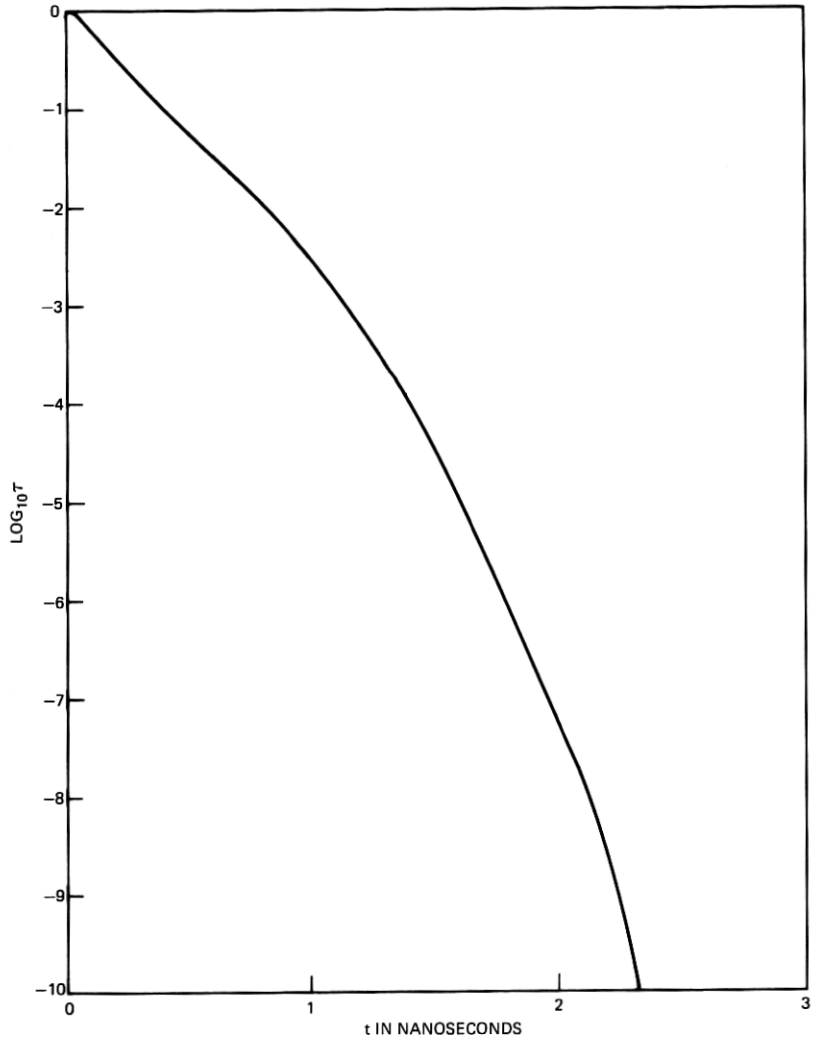

Fig. 9—Plot of $\log_{10} \tau(t)$ as a function of t for the BCCD of Fig. 8.

Strain and Schryer[25] has been adapted to cases such as the present one. Initially, we assumed the plate voltages were the opposite of those shown in Fig. 7, and the charge was all stored in the left-hand well ($5\,\mu \leqq x \leqq 15\,\mu$). Then at $t = 0$, the voltages were instantaneously reversed to the configuration shown in Fig. 7, and the charge flowed from the left-hand well to the right-hand well ($25\,\mu \leqq x \leqq 35\,\mu$). The

calculation[26] based on a one-dimensional analysis of the charge flow in the channel showed that if the well initially contained 10^6 electrons, then essentially *all* the charge transfers in 1.8 ns (see Fig. 9). Let $Q_\varrho(t)$ denote the total charge in the left-hand well at time t, and define the transfer ratio $\tau(t)$ by

$$\tau(t) = Q_\varrho(t)/Q_\varrho(0). \tag{5}$$

Figure 9 plots $\log_{10} \tau(t)$ as a function of t. Figure 10 plots the charge density in the channel (in dimensionless units) as a function of position for $t = 0$, 0.18 ns, and 2.56 ns. By referring to Fig. 8, it is seen that the two deep depressions in the curve for $t = 0.18$ ns are due to the very strong field-aided transfer at those points. Note in Table II that the minimum field under the receiving barrier is 710 V/cm, while the minimum field under the sending well is 1755 V/cm. This accounts for the bunching effect at $t = 0.18$ ns shown in Fig. 10. This bunching effect can be reduced by increasing the most positive electrode potential.

By taking advantage of the capabilities of either self-aligned gate technology or undercut isolation schemes and of ion implantation technologies, the preceding paragraphs have shown the design param-

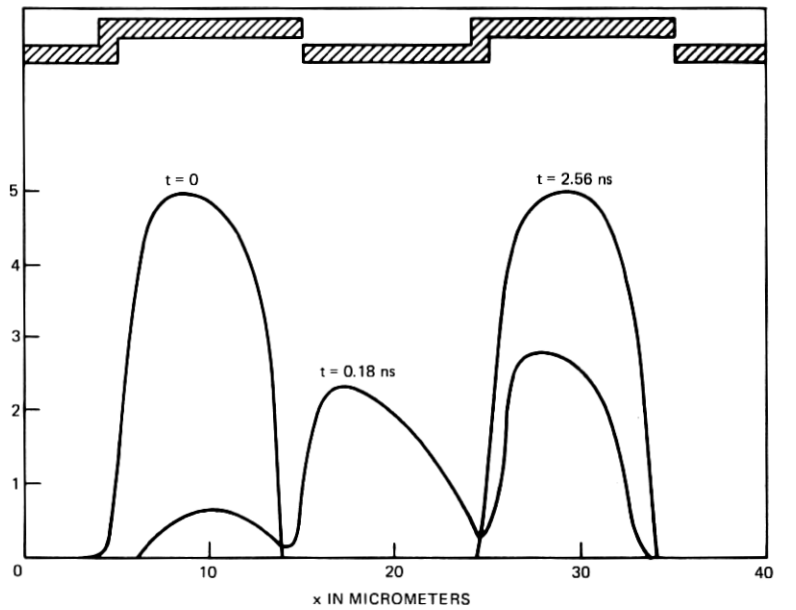

Fig. 10—Charge distribution (in dimensionless units) along the channel for three different times.

eters required in the fabrication of an extremely fast and efficient two-phase, buried-channel, charge-coupled device. This device should have the advantages of convenient operation because of two-phase operation and high transfer efficiency because the buried channel eliminates surface trapping and surface scattering of the transferring carriers and introduces strong fringing fields. Further, by careful design, the charge capacity of this device, while lower, can be competitive with surface devices.

APPENDIX

This appendix briefly derives some results using a simplified, one-dimensional model of a BCCD and the well-known depletion-layer approximation.[20] The oxide layer has thickness d and permittivity ϵ_{0x}. The n-type layer has a thickness Y_1, permittivity ϵ_s, and is *uniformly* doped with donor density N_D. The p-type substrate is assumed to be infinitely thick, with permittivity ϵ_s and acceptor density N_A. The electrostatic potential is denoted by $\varphi(x)$.

We introduce dimensionless quantities as follows. All distances are measured in terms of Debye lengths λ_D,

$$\lambda_D = (\epsilon_s kT/e^2 N_A)^{\frac{1}{2}}, \tag{6}$$

where k is Boltzmann's contant, T is the absolute temperature, and e is the magnitude of the electronic charge. Then we define

$$z = y/\lambda_D, \quad h = d/\lambda_D, \quad z_1 = Y_1/\lambda_D. \tag{7}$$

In addition, we define the dimensionless electrostatic and electrode potentials

$$\psi(z) = e\varphi(y)/kT, \quad V_0 = eV_G/kT, \tag{8}$$

and the dimensionless ratios

$$\eta = \epsilon_{0x}/\epsilon_s, \quad \sigma = N_D/N_A. \tag{9}$$

Then $\psi(y)$ is the solution of the equations

$$\psi''(z) = 0, \qquad 0 \leqq z \leqq h, \tag{10a}$$

$$\psi''(z) = -\sigma, \qquad h \leqq z \leqq h + z_1, \tag{10b}$$

$$\psi''(z) = 1, \qquad h + z_1 \leqq z \leqq h + z_1 + R, \tag{10c}$$

$$\psi(z) \equiv 0, \qquad h + z_1 + R < z, \tag{10d}$$

which satisfies the electrostatic boundary conditions

$$\psi(0) = V_0, \tag{11a}$$

$$\psi(h-) = \psi(h+), \qquad \eta\psi'(h-) = \psi'(h+), \tag{11b}$$

$$\psi(h + z_1-) = \psi(h + z_1+), \qquad \psi'(h + z_1-) = \psi'(h + z_1+), \tag{11c}$$

$$\psi(h + z_1 + R) = \psi'(h + z_1 + r) = 0. \tag{11d}$$

The thickness of the depletion layer, R, is an unknown to be determined from the boundary conditions. The solution can be determined easily.

$$\begin{aligned}
\psi(z) &= V_0 + (\sigma z_1 - R)\frac{z}{\eta}, \qquad 0 \leqq z \leqq h, \\
&= -\tfrac{1}{2}(1 + \sigma)(z - h - z_1)^2 + \tfrac{1}{2}(z - h - z_1 - R)^2, \\
&\qquad\qquad h \leqq z \leqq h + z_1, \\
&= \tfrac{1}{2}(z - h - z_1 - R)^2, \qquad h + z_1 \leqq z \leqq h + z_1 + R,
\end{aligned} \tag{12}$$

where

$$R = -\left(\frac{h}{\eta} + z_1\right) + \sqrt{(1 + \sigma)\left(\frac{h}{\eta} + z_1\right)^2 - \sigma\left(\frac{h}{\eta}\right)^2 + 2V_0}. \tag{13}$$

The electrostatic field is obtained from (12) by differentiation.

To determine the position, y_m, of the electrostatic potential maximum, we first set $\psi'(z_m) = 0$ in $h < z < h + z_1$ and obtain

$$z_m = h + \frac{1}{\sigma}(\sigma z_1 - R) = h + z_1 - \frac{R}{\sigma}. \tag{14}$$

Thus the position of this maximum occurs in $h < z < h + z_1$ if and only if $\sigma z_1 - R > 0$. If $\sigma z_1 - R \leqq 0$, it is easy to show that $\psi(z) \leqq V_0$, and the device would operate as a surface CCD, since the potential maximum in the semiconductor would be at the oxide-semiconductor interface. It is easy to show that $\sigma z_1 - R > 0$ if and only if

$$V_0 < \tfrac{1}{2}\sigma(1 + \sigma)z_1^2. \tag{15}$$

When it is written in terms of dimensional quantities, we obtain inequality (2).

Inequality (15) is a rough criterion that places an upper limit on the plate voltages that may be used in a BCCD.

Assuming (15) is satisfied, the value of the electrostatic potential maximum is

$$\psi(z_m) = \frac{1}{2}\left(1 + \frac{1}{\sigma}\right)R^2. \tag{16}$$

It is straightforward to show that

$$\frac{dR}{dh} = \frac{\sigma z_1 - R}{h + \eta(R + z_1)}. \tag{17}$$

Thus, as long as $\sigma z_1 - R > 0$, $dR/dh > 0$. Consequently, from (16) $d\psi(z_m)/dh > 0$ as long as (15) is satisfied. In other words, for electrode voltages within the operating range of a BCCD, the value of the electrostatic potential maximum is greater under the thick-oxide step than it is under the thin-oxide step. This is just the opposite of the case in a surface, stepped-oxide CCD. From (14) it follows that

$$\frac{d}{dh}(z_m - h) = -\frac{1}{\sigma}\frac{dR}{dh}. \tag{18}$$

Thus, within the operating range, the position of the electrostatic maximum is closer to the oxide-semiconductor interface under the thick-oxide step than it is under the thin-oxide step.

REFERENCES

1. R. H. Walden, R. H. Krambeck, R. J. Strain, J. McKenna, N. L. Schryer, and G. E. Smith, "The Buried Channel Charge Coupled Device," B.S.T.J., *51*, No. 7 (September 1972), pp. 1635–1640. Also presented at the Device Research Conference, Ann Arbor, Mich., June 1971.
2. L. J. M. Esser, "Peristaltic Charge-Coupled Device: A New Type of Charge-Transfer Device," Elec. Ltrs., *8*, No. 25 (December 1973), pp. 620–621.
3. C. K. Kim, J. M. Early, and G. F. Amelio, "Buried Channel Charge Coupled Devices," Conference Proceedings NEREM, Part 1 (October 1972), pp. 161–164.
4. C. C. Kim and R. H. Dyck, "Low Light Level Imaging With Buried Channel Charge Coupled Devices," Proc. IEEE, *61*, No. 8 (August 1973), pp. 1146–1147.
5. K. C. Gunsager, C. K. Kim, and J. D. Phillips, "Performance and Operation of Buried Channel Charge Coupled Devices," IEDM Washington, Technical Digest (December 1973), pp. 21–23.
6. L. J. M. Esser, M. G. Collet, and J. G. von Sonten, "The Peristaltic Charge Coupled Device," IEDM Washington, Technical Digest (December 1973), pp. 17–20.
7. R. H. Krambeck, R. H. Walden, and K. A. Pickar, "Implanted-Barrier, Two-Phase Charge-Coupled Devices," Appl. Phys. Ltrs., *19*, No. 12 (December 1971), pp. 520–522.
8. R. H. Krambeck, R. H. Walden, and K. A. Pickar, "A Doped Surface Two-Phase CCD," B.S.T.J., *51*, No. 8 (October 1972), pp. 1849–1866.
9. W. F. Kosnocky and J. E. Carnes, "Charge Coupled Digital Circuits," IEEE J. Solid State Circuits, *SC-6*, No. 2 (October 1971), pp. 314–322.
10. C. N. Berglund, R. J. Powell, E. H. Nicollian, and J. T. Clemens, "Two-Phase Stepped Oxide CCD Shift Register Using Undercut Isolation," Appl. Phys. Ltrs., *20*, No. 11 (June 1972), pp. 413–414; C. N. Berglund, E. H. Nicollian, and J. T. Clemens, "Undercut Isolation—A Technique for Closely Spaced and Self-Aligned Metallization Patterns for Integrated Circuits," J. Electrochem. Soc., *120*, No. 9 (September 1973), pp. 1255–1260.
11. W. E. Engeler, J. J. Tiemann, and R. D. Baertsch, "Surface Charge Transport in Silicon," Appl. Phys. Ltrs., *17*, No. 11 (December 1970), pp. 469–472.

12. D. Kahng and E. H. Nicollian, "Monolith Semiconductor Apparatus Adapted for Sequential Charge Transfer," U. S. Patent 3, 651, 349, applied for February 16, 1970, issued March 21, 1972.
13. J. McKenna and N. L. Schryer, "The Potential in a Charge-Coupled Device With No Mobile Minority Carriers," B.S.T.J., *52*, No. 10 (December 1973), pp. 1765–1793.
14. J. McKenna and N. L. Schryer, "The Potential in a Charge Coupled Device With No Mobile Minority Carriers and Zero Plate Separation," B.S.T.J., *52*, No. 5 (May–June 1973), pp. 669–696.
15. W. J. Bertram, A. M. Mohsen, F. J. Morris, D. A. Sealer, C. H. Sequin, and M. F. Tompsett, "A Three-Level Metallization Three Phase CCD," IEDM Late News Paper (1973).
16. R. H. Walden, "Buried Channel Charge Coupled Apparatus," U. S. Patent applied for, April 27, 1973.
17. A. M. Mohsen, R. Bower, and T. C. McGill, "Overlapping-Gate Buried Channel Charge Coupled Device," Elec. Ltrs., *9*, No. 17 (August 1973), pp. 396–398.
18. D. M. Erb, W. Kotyczka, S. C. Su, C. Wong, and G. Clough, "An Overlapping Electrode Buried Channel CCD," IEDM Washington, Technical Digest (December 1973), pp. 24–25.
19. A. S. Grove, "Physics and Technology of Semiconductor Devices," New York: John Wiley, 1967, pp. 49–50.
20. J. McKenna and N. L. Schryer, "On the Accuracy of the Depletion Layer Approximation for Charge Coupled Devices," B.S.T.J., *51*, No. 7 (September 1972), pp. 1471–1485.
21. M. Abramowitz and J. A. Stegun, "Handbook of Mathematical Functions," Washington, D. C.: National Bureau of Standards, 1964, p. 297.
22. L. J. M. Esser, "The Peristaltic Charge-Coupled Device for High Speed Charge Transfer," ISSCC Philadelphia Digest of Technical Papers (February 1974), pp. 28–29.
23. N. L. Schryer, unpublished work.
24. W. H. Kent, "Charge Distribution in Buried-Channel Charge-Coupled Devices," B.S.T.J., *52*, No. 6 (July–August 1973), pp. 1009–1024.
25. R. J. Strain and N. L. Schryer, "A Nonlinear Diffusion Analysis of Charge-Coupled-Device Transfer," B.S.T.J., *50*, No. 6 (July–August 1971), pp. 1721–1740.
26. N. L. Schryer and J. McKenna, "An Analysis of Field-Aided Charge-Coupled Device Transfer," unpublished work.